Abstract of the Disclosure

A multi-level EEPROM cell and a method of manufacture thereof are provided so as to improve a program characteristic of the multi-level cell. For the purpose, the multi-level flash EEPROM cell includes a floating gate formed as being electrically separated from a silicon substrate by an underlying tunnel oxide layer, a first dielectric layer formed over the top of the floating gate, a first control gate formed on the floating gate as being electrically separated from the floating gate by the first dielectric layer, a second dielectric layer formed on the sidewall and top of the first control gate, a second control gate formed on the sidewall and top of the first control gate as being electrically separated from the first control gate by the second dielectric layer, and a source and drain formed in the substrate as being self-aligned with both edges of the second control gate.